ABSTRACT OF THE DISCLOSURE

A data transfer unit (13) is provided for use in a clock swapping system which controls data transfer with a data transmission permit signal (rwo) and data reception permit signal (rro). The data transfer unit (13) includes a data latch (21) which latches transfer data in time with a transmission enable signal (ewi) and from which the data is read in time with a reception enable signal (eri), a first FR-FF circuit (31) which delays the transmission enable signal (ewi) for at least one period of a transmission clock (ckw), and a third SR-FF circuit 33 which delays the reception enable signal (eri) for a period of a reception clock (ckr). In the data transfer unit (13), a signal latched by the first SR-FF circuit (31) is latched a series of two times in time with the reception clock (ckr) to generate the reception permit signal (rro) and a signal latched by the third SR-FF circuit (33) is latched a series of two times in time with the transmission clock (ckw) to generate the transmission permit signal (rwo). Thus, the data transfer unit (13) can always assure stable data transfer by eliminating influence of a metastable state, if any.